

Cambridge International AS & A Level**COMPUTER SCIENCE****9618/12****Paper 1 Theory Fundamentals****May/June 2025****Excel in Your O & A Level Studies****Get expert Online Tuition and Comprehensive Past Paper Solutions for Cambridge O & A Levels**

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- 1 (a) The table has six statements about the Von Neumann model for a computer system. Three of the statements are incorrect.

Statement number	Statement
1	The Program Counter (PC) stores the next instruction to be fetched from memory.
2	The Arithmetic and Logic Unit (ALU) performs mathematical and logical operations.
3	The Control Unit (CU) sends signals to other components on the data bus.
4	The Memory Data Register (MDR) transfers data to the memory address stored in the Memory Address Register (MAR).
5	The MAR stores an address from memory.
6	The Accumulator (ACC) stores the result of calculations.

Complete the table by writing the **three** incorrect statement numbers and the corrected statements.

Incorrect statement number	Corrected statement
.....	
.....	
.....	

- (b) Registers that are used in the Fetch-Execute (F-E) cycle include the PC, MAR, MDR and the ACC.

Identify **one** other register and describe its role in the Fetch-Execute (F-E) cycle.

Register

Role

- (c) Explain how an interrupt from an input device will be detected and handled in the F-E cycle.

.....

Solution:

(a)

Incorrect statement number	Corrected statement
1	The Program Counter (PC) stores the memory address of the next instruction to be fetched from memory. It does not store the instruction itself.
3	The Control Unit (CU) sends control signals to other components using the control bus. The data bus transfers data, not control signals.
4	The Memory Data Register (MDR) stores data being transferred to or from memory. The MAR stores the memory

(b)

Register: Current Instruction Register (CIR)

Role: Stores the current instruction fetched from memory so that the Control Unit can decode and execute it.

(c)

1. An **input device** (such as a keyboard or mouse) sends an **interrupt signal** to the CPU when it needs attention.
2. At the **end of each Fetch-Execute (F-E) cycle**, the **Control Unit (CU)** checks whether any interrupt requests are waiting.
3. If **no interrupt** is detected, the CPU continues executing the next instruction in the program.

4. If an **interrupt is detected**, the CPU first **completes the current instruction** before responding to the interrupt.
5. The CPU **saves the current state** of the running program (such as the contents of registers and the Program Counter) in memory or on the stack so that execution can resume later.